IN THE CLAIMS

Please cancel Claims 1, 2, 8-10, and 17-23 without prejudice or disclaimer.

Claims 1 and 2 (cancelled).

Claim 3 (currently amended): An integrated circuit comprising:

a closed loop amplifier circuit containing an operational amplifier with a finite gain; and

a correction circuit correcting an error in an output of said closed loop amplifier,

~~The integrated circuit of claim 1,~~ wherein said correction circuit comprises a feedback impedance and an reference impedance of a first ratio, wherein said first ratio is determined by adjusting a desired amplification factor according to said error.

Claim 4 (currently amended): An integrated circuit comprising:

a closed loop amplifier circuit containing an operational amplifier with a finite gain; and

a correction circuit correcting an error in an output of said closed loop amplifier,

wherein said correction circuit comprises a feedback impedance and an reference impedance of a first ratio, wherein said first ratio is determined by adjusting a desired amplification factor according to said error, and

~~The integrated circuit of claim 3,~~ wherein said first ratio equals ((F-1) (1+factor)), wherein F equals the desired amplification factor for said closed loop amplifier circuit

and said factor equals ((1/A1 + 1/A2) x (1 + Z1/Z2) / 2), wherein said finite gain varies between A1 and A2.

Claim 5 (currently amended): The integrated circuit of claim ~~1~~ 3, wherein said closed loop amplifier circuit receives an analog input signal and generates an analog output signal as said output, said integrated circuit further comprising:

an analog to digital converter (ADC) converting a sample of said analog output signal to an intermediate digital code,

wherein said correction circuit corrects said error by performing a mathematical operation on said intermediate digital code to generate a corrected digital code representing said output corrected for said error.

Claim 6 (currently amended): An integrated circuit comprising:

a closed loop amplifier circuit containing an operational amplifier with a finite gain; and

a correction circuit correcting an error in an output of said closed loop amplifier,

wherein said closed loop amplifier circuit receives an analog input signal and generates an analog output signal as said output, said integrated circuit further comprising:

an analog to digital converter (ADC) converting a sample of said analog output signal to an intermediate digital code,

wherein said correction circuit corrects said error by performing a mathematical operation on said intermediate digital code to generate a corrected digital code representing said output corrected for said error, and

~~The integrated circuit of claim 5,~~ wherein said intermediate digital code comprises a plurality of sub-codes (V1, V2, ... Vn) generated by a corresponding plurality of sub-ADCs contained in said ADC, wherein said closed loop amplifier circuit is contained in a first stage generating said V1, said mathematical operation comprises:

multiplying a value formed by (V2, .. Vn) by (1+Factor), wherein Factor equals (F/A), A equals sad finite gain.

Claim 7 (currently amended): The integrated circuit of claim ~~1~~ 3, wherein said correction circuit divides said output by (1 - 1/A), wherein A equals said finite gain, to correct said error.

Claims 8-10 (cancelled).

Claim 11 (currently amended): An analog to digital converter (ADC) converting a sample of an analog signal to a digital code, said ADC comprising:

a plurality of stages, each of said plurality of stages generating a corresponding one of a plurality of sub-codes, each of said plurality of sub-codes containing at least one bit, wherein said sub-codes are used to generate said digital code, at least one of said plurality of stages comprising:

a sub-ADC receiving an input signal and generating a corresponding one of said plurality of sub-codes representing a strength of said input signal;

a digital to analog converter (DAC) converting said corresponding one of said plurality of sub-codes to a corresponding intermediate signal;

an subtractor subtracting said corresponding intermediate signal from said input signal to generate an subtractor output; and

a closed loop amplifier containing an operational amplifier with a finite gain, said closed loop amplifier amplifying said subtractor output to generate said input signal for a next stage; and

a correction circuit correcting an error in an output of said closed loop amplifier,

~~The ADC of claim 9,~~ wherein said correction circuit comprises a feedback impedance and an reference impedance having impedance of a first ratio, wherein said first ratio is determined by adjusting a desired amplification factor according to said error.

Claim 12 (currently amended): An analog to digital converter (ADC) converting a sample of an analog signal to a digital code, said ADC comprising:

a plurality of stages, each of said plurality of stages generating a corresponding one of a plurality of sub-codes, each of said plurality of sub-codes containing at least one bit, wherein said sub-codes are used to generate said digital code, at least one of said plurality of stages comprising:

a sub-ADC receiving an input signal and generating a corresponding one of said plurality of sub-codes representing a strength of said input signal;

a digital to analog converter (DAC) converting said corresponding one of said plurality of sub-codes to a corresponding intermediate signal;

an subtractor subtracting said corresponding intermediate signal from said input signal to generate an subtractor output; and

a closed loop amplifier containing an operational amplifier with a finite gain, said closed loop amplifier amplifying said subtractor output to generate said input signal for a next stage; and

a correction circuit correcting an error in an output of said closed loop amplifier,

wherein said correction circuit comprises a feedback impedance and an reference impedance having impedance of a first ratio, wherein said first ratio is determined by adjusting a desired amplification factor according to said error, and

~~The ADC of claim 11,~~ wherein said first ratio equals ((F-1) (1+factor)), wherein F equals the desired amplification factor for said closed loop amplifier circuit and said factor equals ((1/A1 + 1/A2) x (1 + Z1/Z2) / 2), wherein said finite gain varies between A1 and A2.

Claim 13 (currently amended): The ADC of claim ~~8~~ 11, wherein said closed loop amplifier circuit receives an analog input signal and generates an analog output signal as said output, said ADC further comprising:

an analog to digital converter (ADC) converting a sample of said analog output signal to an intermediate digital code,

wherein said correction circuit corrects said error by performing a mathematical operation using said intermediate digital code to generate a corrected digital code representing said output corrected for said error.

Claim 14 (original): The ADC of claim 13, wherein said intermediate digital code comprises a plurality of sub-codes (V1, V2, ... Vn) generated by a corresponding plurality of sub-ADCs, wherein said closed loop amplifier circuit is contained in a first stage generating said V1, said mathematical operation comprises:

multiplying a value formed by (V2, .. Vn) by (1+Factor).

Claim 15 (currently amended): The ADC of claim ~~8~~ 11, wherein said correction circuit divides said output by (1 - 1/A), wherein A equals said finite gain, to correct said error.

Claim 16 (currently amended): The ADC of claim ~~8~~ 11, wherein said sub-ADC comprises a flash ADC.

Claims 17-23 (cancelled).

Claim 24 (currently amended): The device of claim ~~23~~ 26, wherein said finite gain is low such that said ADC operates to provide a high throughput performance, and wherein said correction circuit reduces said error caused by use of said operational amplifier with low finite gain.

Claim 25 (currently amended): The device of claim ~~23~~ 26, wherein said finite gain is smaller than at least 6 x (N-1), wherein N represents a number of bits contained in said digital code.

Claim 26 (currently amended): A device comprising:

an analog to digital converter (ADC) converting a sample of an analog signal to a digital code, said ADC comprising:

a plurality of stages, each of said plurality of stages generating a corresponding one of a plurality of sub-codes, each of said plurality of sub-codes containing at least one bit, at least one of said plurality of stages comprising:

a sub-ADC receiving an input signal and generating a corresponding one of said plurality of sub-codes representing a strength of said input signal;

a digital to analog converter (DAC) converting said corresponding one of said plurality of sub-codes to a corresponding intermediate signal;

an subtractor subtracting said corresponding intermediate signal from said input signal to generate an subtractor output; and

a closed loop amplifier containing an operational amplifier with a finite gain, said closed loop amplifier amplifying said subtractor output to generate said input signal for a next stage;

a correction circuit correcting an error in an output of said closed loop amplifier,

~~The device of claim 24,~~ wherein said correction circuit comprises a feedback impedance and an reference impedance having resistance of a first ratio, wherein said

first ratio is determined by adjusting a desired amplification factor according to said error.

Claim 27 (currently amended): A device comprising:

an analog to digital converter (ADC) converting a sample of an analog signal to a digital code, said ADC comprising:

a plurality of stages, each of said plurality of stages generating a corresponding one of a plurality of sub-codes, each of said plurality of sub-codes containing at least one bit, at least one of said plurality of stages comprising:

a sub-ADC receiving an input signal and generating a corresponding one of said plurality of sub-codes representing a strength of said input signal;

a digital to analog converter (DAC) converting said corresponding one of said plurality of sub-codes to a corresponding intermediate signal;

an subtractor subtracting said corresponding intermediate signal from said input signal to generate an subtractor output; and

a closed loop amplifier containing an operational amplifier with a finite gain, said closed loop amplifier amplifying said subtractor output to generate said input signal for a next stage;

a correction circuit correcting an error in an output of said closed loop amplifier,

wherein said correction circuit comprises a feedback impedance and an reference impedance having resistance of a first ratio, wherein said first ratio is determined by adjusting a desired amplification factor according to said error, and

~~The device of claim 26,~~ wherein said first ratio equals ((F-1) (1+factor)), wherein F equals the desired amplification factor for said closed loop amplifier circuit and said factor equals ((1/A1 + 1/A2) x (1 + Z1/Z2) / 2), wherein said finite gain varies between A1 and A2.

Claim 28 (currently amended): The device of claim ~~23~~ 26, wherein said closed loop amplifier circuit receives an analog input signal and generates an analog output signal as said output, said ADC further comprising:

an analog to digital converter (ADC) converting a sample of said analog output signal to an intermediate digital code,

wherein said correction circuit corrects said error by performing a mathematical operation using said intermediate digital code to generate a corrected digital code representing said output corrected for said error.

Claim 29 (original): The device of claim 28, wherein said intermediate digital code comprises a plurality of sub-codes (V1, V2, ... Vn) generated by a corresponding plurality of sub-ADCs, wherein said closed loop amplifier circuit is contained in a first stage generating said V1, said mathematical operation comprises:

multiplying a value formed by (V2, .. Vn) by (1+Factor).

Claim 30 (currently amended): The device of claim ~~23~~ 26, wherein said correction circuit divides said output by (1 - 1/A) to correct said error, wherein A equals said finite gain.

Claim 31 (currently amended): The device of claim ~~23~~ 26, wherein said device comprises a wireless base station.